IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

Claims 1-6 (Canceled)

7. (Currently amended) A method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising the steps of:

forming a device isolation ~~film in a given region on~~ structure in a semiconductor substrate ~~to define an active region and a device isolation region~~;

~~defining said active region into a cell region and a peripheral circuit region by a given process;~~

forming a tunnel oxide ~~film~~ layer and ~~a first polysilicon film on the entire structure including the device isolation film and then patterning said tunnel oxide film and said first polysilicon film so that said tunnel oxide film and said first polysilicon film remain in a given region of said cell region, thus defining~~ a floating gate layer in the peripheral region of the semiconductor substrate;

~~sequentially forming an insulating film and a second polysilicon film on the entire structure including said cell region and said peripheral circuit region, the insulating film~~ a dielectric layer and a control gate layer over the floating gate layer in the cell region and over the semiconductor substrate in the peripheral region, the dielectric layer including an oxide ~~film~~ layer and a nitride layer ~~film and being formed under the second polysilicon film~~; and

~~patterning said second polysilicon film and said insulating film so that they can remain only in a given region of said cell region and said peripheral circuit region respectively, thus forming a control gate of the flash memory cell on the insulating film covering the floating~~

~~gate in said cell region respectively, and a gate of the code address memory cell on the insulating film covering a surface of the substrate in said peripheral circuit region; and~~

~~performing~~ forming a source and a drain region in the semiconductor substrate by performing an impurity ion implantation process ~~for a given region of said semiconductor substrate to form a source region and a drain region, so that a flash memory cell including the tunnel oxide film, the first polysilicon film, the insulating film and the second polysilicon film is formed in said cell region, and a code address memory cell including the insulating film and the second polysilicon film is formed in said peripheral circuit region~~.

8. (Currently amended) The method of manufacturing ~~a~~ the code address memory cell in the peripheral region and the flash memory cell in the cell region according to claim 7, wherein ~~said insulating film~~ the dielectric layer is formed by stacking at least two or more layers of at least one of ~~said~~ the oxide ~~film~~ layer and ~~said insulating film~~ the nitride layer.

9. (Currently amended) The method of manufacturing ~~a~~ the code address memory cell in the peripheral region and the flash memory cell in the cell region according to claim 7, wherein ~~said insulating film has a~~ the dielectric layer is formed in thickness of about 30~300Å.

10. (Currently amended) The method of manufacturing ~~a~~ the code address memory cell in the peripheral region and the flash memory cell in the cell region according to claim 7, wherein ~~said insulating film has a~~ the dielectric layer is formed by stacking a first oxide ~~film~~ layer, a nitride ~~film~~ layer and a second oxide ~~film~~ layer.

11. (Currently amended) The method of manufacturing ~~a~~ the code address memory cell in the peripheral region and the flash memory cell in the cell region according to

claim 7, wherein ~~said insulating film has a~~ the dielectric layer is formed by stacking a first oxide ~~film~~ layer, a first nitride ~~film~~ layer, a second oxide ~~film~~ layer and a second nitride ~~film~~ layer.

12. (Currently amended) The method of manufacturing ~~a~~ the code address memory cell in the peripheral region and the flash memory cell in the cell region according to claim 7, wherein ~~said insulating film has a~~ the dielectric layer is formed by stacking a first oxide ~~film~~ layer, a first nitride ~~film~~ layer, a second oxide ~~film~~ layer, a second nitride ~~film~~ layer and a third oxide ~~film~~ layer.

13. (Currently amended) A method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising the steps of:

forming a device isolation ~~film in a given region on~~ structure in a semiconductor substrate ~~to define an active region and a device isolation region;~~

~~defining said active region into a cell region and a peripheral circuit region by a given process;~~

forming a tunnel oxide ~~film~~ layer and ~~a first polysilicon film on the entire structure including the device isolation film and then patterning said tunnel oxide film and said first polysilicon film so that said tunnel oxide film and said first polysilicon film remain in a given region of said cell region, thus defining~~ a floating gate layer in the peripheral region of the semiconductor substrate;

~~sequentially~~ forming ~~an insulating film and a second polysilicon film on the entire structure including said cell region and said peripheral circuit region, wherein said insulating film is formed by stacking~~ a dielectric layer and a control gate layer over the floating gate in the cell region and over the semiconductor substrate in the peripheral region, the dielectric

layer including a first oxide ~~film~~ layer, a first nitride ~~film~~ layer, a second oxide ~~film~~ layer, a second nitride ~~film~~ layer and a third oxide ~~film~~ layer;

~~patterning said second polysilicon film and said insulating film so that they can remain only in a given region of said cell region and said peripheral circuit region respectively, thus forming a control gate of the flash memory cell on the insulating film covering the floating gate in said cell region respectively, and a gate of the code address memory cell on the insulating film covering a surface of the substrate in said peripheral circuit region; and~~

~~performing~~ forming a source and a drain region in the semiconductor substrate by performing an impurity ion implantation process ~~for a given region of said semiconductor substrate to form a source region and a drain region, so that a flash memory cell including the tunnel oxide film, the first polysilicon film, the insulating film and the second polysilicon film is formed in said cell region, and a code address memory cell including the insulating film and the second polysilicon film is formed in said peripheral circuit region.~~

14. (New) The method of manufacturing the code address memory cell in the peripheral region and the flash memory cell in the cell region according to claim 7, the floating gate layer and the control gate layer is formed of polysilicon.

15. (New) The method of manufacturing the code address memory cell in the peripheral region and the flash memory cell in the cell region according to claim 13, the floating gate layer and the control gate layer is formed of polysilicon.